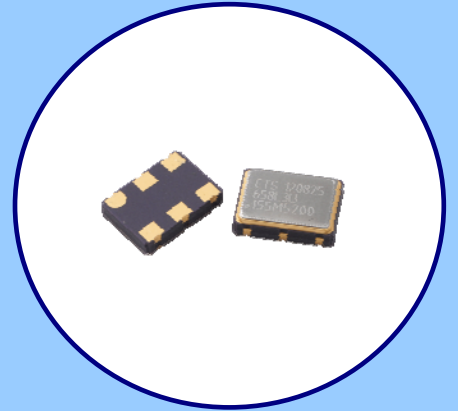


LVPECL OR LVDS CLOCK OSCILLATOR

FEATURES

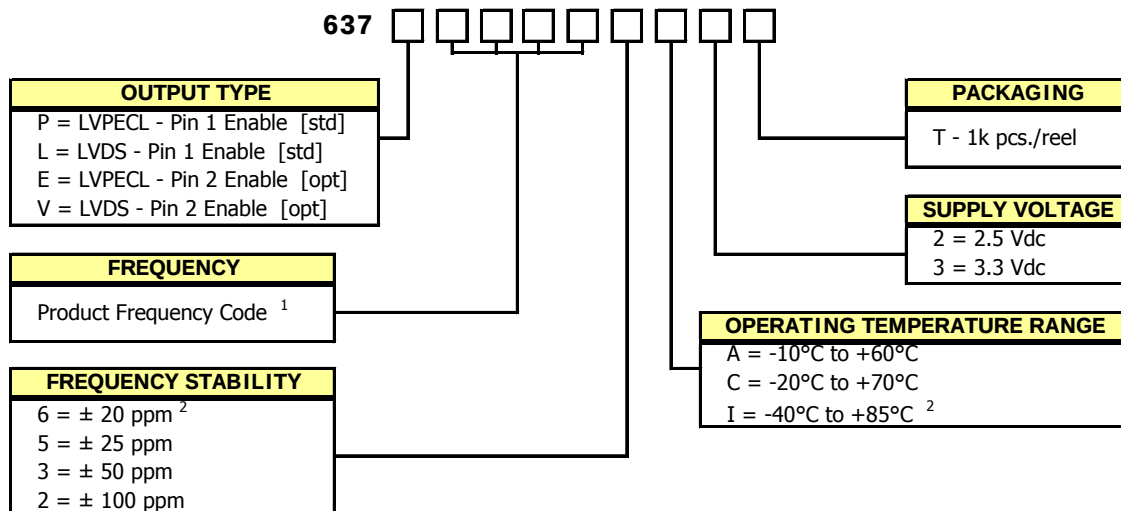
- Standard 7.0mm x 5.0mm, 6-Pad Surface Mount Package
- **Low Phase Jitter, 0.5ps RMS Maximum**
- LVPECL or LVDS Output
- Fundamental and 3rd Overtone Crystal Designs
- Frequency Range 19.44 – 320 MHz
- Frequency Stability ± 50 ppm Standard
- Operating Voltages +2.5Vdc or +3.3Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



APPLICATIONS

Model 637 is ideal for applications such as broadband access, SerDes, Ethernet/Gigabit Ethernet, SONET/SDH and optical networking.

ORDERING INFORMATION



1] Refer to document 016-1454-0, Frequency Code Tables.

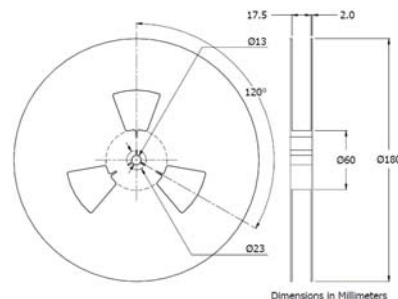
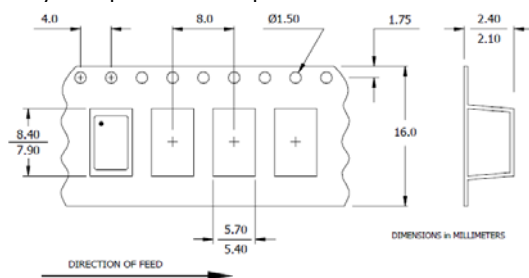
3-digits required for frequencies below 100MHz and 4-digits for frequencies 100MHz or greater.

2] Consult factory for availability of 6I Stability/Temperature combination.

**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. maximum per 180mm reel.



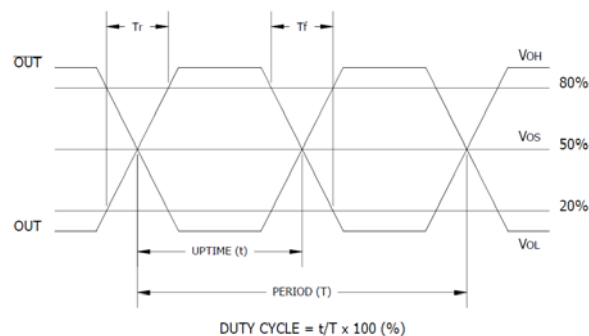
ELECTRICAL CHARACTERISTICS

ELECTRICAL PARAMETERS	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Storage Temperature	T_{STG}	-	-40	-	+100	°C
	Frequency Range	f_0	-	19.44	-	320	MHz
	LVPECL						
	LVDS						
	Frequency Stability	$\Delta f/f_0$	All Inclusive, see Note 1.	-	-	20, 25, 50, 100	± ppm
			1st year aging	-	-	3	
	Operating Temperature	T_A	-	-20	25	+70	°C
	Commercial						
	Industrial			-40		+85	
	Supply Voltage	V_{CC}	± 5 %	2.38	2.5	2.63	V
				3.14	3.3	3.47	
	Supply Current	I_{CC}	Maximum Load	-	-	88	mA
	LVPECL						
	LVDS			-	-	65	
	Start Up Time	T_S	Application of V_{CC}	-	2	5	ms
	Phase Jitter	t_{jrms}	Bandwidth 12 kHz - 20 MHz	-	0.3	0.5	ps
	Period Jitter RMS	p_{jrms}	-	-	2.1	-	
	Period Jitter Pk-Pk		-	-	22	-	
	Enable Function		Standby				V
	Enable Input Voltage	V_{IH}	Pin 1 or 2 Logic '1', Output Enabled	$0.7 \cdot V_{CC}$	-	-	
	Disable Input Voltage	V_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	-	$0.3 \cdot V_{CC}$	
	Disable Time	T_{PLZ}	Pin 1 or 2 Logic '0', Output Disabled	-	-	200	ns
	Enable Time	T_{PLZ}	Pin 1 or 2 Logic '1', Output Enabled	-	-	2	ms
	LVPECL WAVEFORM						
	Output Load	R_L	Terminated to $V_{CC} - 2.0V$	-	50	-	Ohms
	Output Duty Cycle	SYM	@ $V_{CC} - 1.3V$	45	-	55	%
	Output Voltage Levels	V_{OH} V_{OL}	PECL Load, -20°C to +70°C	$V_{CC} - 1.025$	-	$V_{CC} - 0.880$	V
	Logic '1' Level		PECL Load, -20°C to +70°C	$V_{CC} - 1.810$	-	$V_{CC} - 1.620$	
	Logic '0' Level	V_{OH} V_{OL}	PECL Load, -40°C to +85°C	$V_{CC} - 1.085$	-	$V_{CC} - 0.880$	V
	Logic '1' Level		PECL Load, -40°C to +85°C	$V_{CC} - 1.830$	-	$V_{CC} - 1.555$	
	Logic '0' Level						
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	0.3	0.7	ns
	LVDS WAVEFORM						
	Output Load	R_L	Between Outputs	-	100	-	Ohms
	Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
	Differential Output Voltage	V_{OD}	$R_L = 100$ Ohms	247	350	454	mV
	Offset Voltage	V_{OS}	LVDS Load	1.125	1.25	1.375	V
	Output Voltage Levels	V_{OH} V_{OL}	LVDS Load	-	1.43	1.6	V
	Logic '1' Level		LVDS Load	0.9	1.1	-	
	Logic '0' Level						
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	0.4	0.7	ns

Notes:

- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

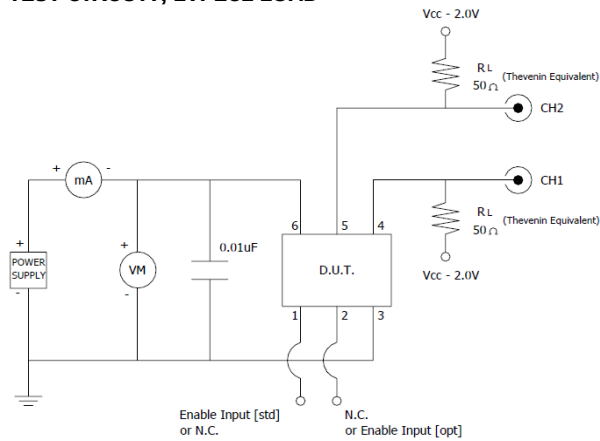
LVPECL/LVDS OUTPUT WAVEFORM



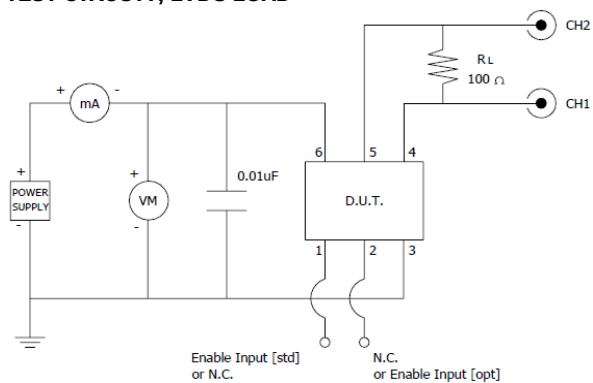
ENABLE TRUTH TABLE

PIN 1 or Pin 2	PIN 4 & 5
Logic '1'	Output
Open	Output
Logic '0'	High Z

TEST CIRCUIT, LVPECL LOAD

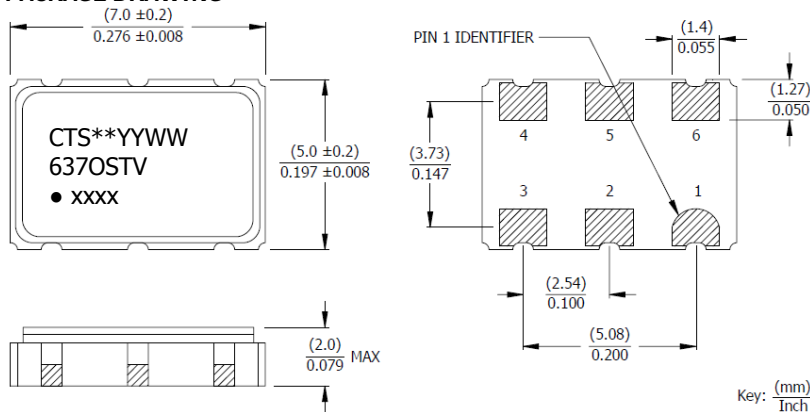


TEST CIRCUIT, LVDS LOAD



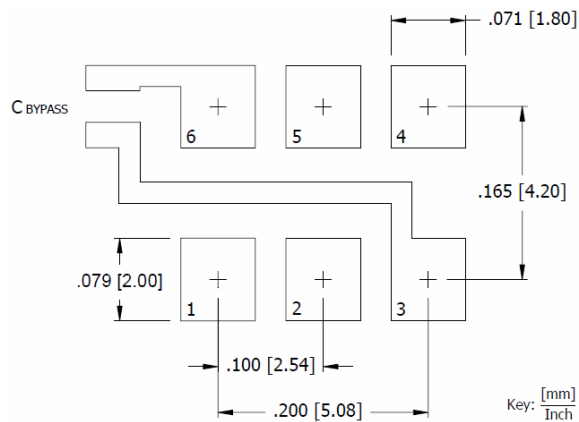
MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be $\geq 0.01 \mu\text{F}$.



MARKING INFORMATION

1. ** - Manufacturing Site Code.
 2. YYWW – Date code, YY – year, WW – week.
 3. O – Output Type. P or E = LVPECL, L or V = LVDS.
 4. ST – Frequency stability/temperature code.
[Refer to Ordering Information.]
 5. V – Voltage code. 3 = 3.3V, 2 = 2.5V
 6. xxxx – Frequency Code.
3-digits, frequencies below 100MHz
4-digits, frequencies 100MHz or greater.
- Refer to document 016-1454-0, Frequency Code Tables.

NOTES

1. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.
2. Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
3. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
4. MSL = 1.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V _{CC}	Supply Voltage